A Low Energy Injection-Locked FSK Transceiver With Frequency-to-Amplitude Conversion for Body Sensor Applications

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***Abstract*—An energy-efficient 920 MHz FSK transceiver for wireless body sensor network (BSN) applications is implemented in 0.18 μm CMOS technology with 0.7 V supply. A transceiver architecture based on injection-locked frequency divider (ILFD) is proposed for the low energy consumption. In the receiver, the ILFD in the signal path converts the received FSK signal to amplitude-modulated signal which is applied to the next envelope detector. In the transmitter, the ILFD is used as digitally-controlled oscillator (DCO) which directly modulates the FSK signal with digital data. The DCO replaces the frequency synthesizer to eliminate the crystal oscillator (XO), which leads to reduce power consumption and cost. The transceiver can detect whether injection locking occurs or not, and calibrates the frequency drift of DCO over temperature variation thanks to ILFD based architecture. The receiver and transmitter consume 420 μW and 700 μW, respectively, at -10 dBm output power with a data rate of 5 Mb/s, corresponding to energy consumption of 84 pJ per received bit and 140 pJ per transmitted bit.**

***Index Terms*—Body sensor network, energy efficient, frequency calibration, frequency-to-amplitude conversion, FSK, injection locked frequency divider, injection locking, low energy, low power, sensor network, transceivers.**

I. Introduction

THE emerging area of wearable or implantable body sensor network (BSN) provides wireless connectivity among various physiological sensors and medical devices [1]. The major design challenge associated with these sensor applications is to extend lifetime of sensor nodes under limited energy sources. Therefore, low energy wireless technologies have been an active research area [2]–[5]. Since the energy consumption is the power consumption multiplied by its usage time, low power transceiver with fast turn-on time should be employed under tight duty cycle control. In addition, body sensor applications such as capsule endoscope, neuro-stimulator, or drug delivery devices require data rate up to 5 Mb/s as discussed in the IEEE 802.15.6 task group for BAN standardization [6].

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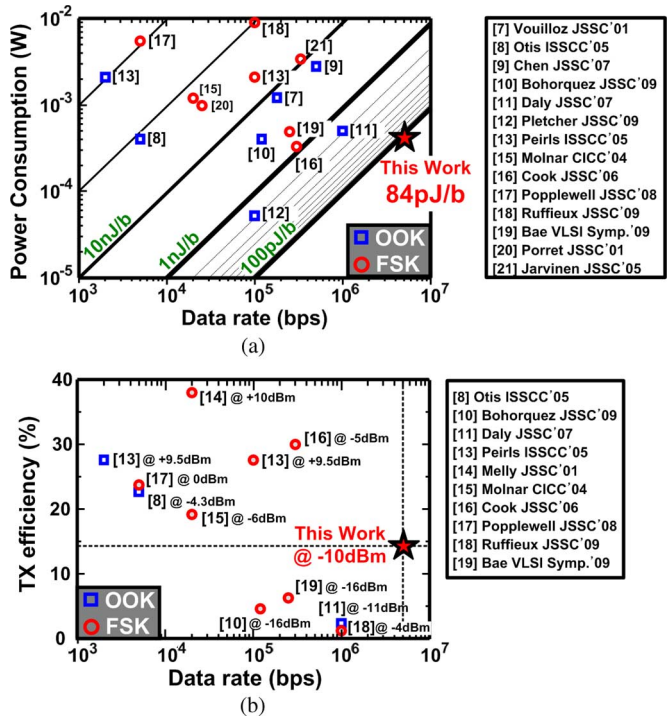

Fig. 1. Trend in recent energy-efficient transceiver. (a) Power consumption and data rate of receiver. (b) Efficiency and data rate of transmitter.

The choice of modulation scheme has significant effects on the transceiver design and the transceiver architecture, which have to remain as simple as possible for low energy consumption. Therefore, it is common that the transceiver trades off spectral efficiency for energy efficiency. There have been two modulation schemes widely used in energy-efficient transceivers for sensor networks. One is on-off-keying (OOK) and the other frequency-shift-keying (FSK), which can be detected by non-coherent architecture thanks to their phase-independent property and low hardware cost, as summarized in Fig. 1.

Fig. 1(a) describes the power consumption and data rate of the recent receivers for sensor applications with energy/bit performance. With the graph of Fig. 1(a), in the receiver side, OOK has the advantage over FSK because it is suitable for simple super-regenerative [7]–[10] and envelope detection [11]–[13] architecture. The extraordinary gain and simplicity of super-regeneration promise low cost and low power consumption. Owing to mitigated sensitivity and selectivity requirements of receiver, envelope detector with just RF amplification and without power-hungry local oscillator (LO) can be the simplest

receiver architecture and leads to the best energy-efficient receiver architecture. However, in transmitter side OOK is strongly susceptible to interferers and requires linear PA to send an amplitude-modulated signal [8], [11]. Moreover, the transmitter's bias points and oscillator must settle in less than a single bit period, potentially limiting data rates. On the other hand, FSK has the merit of transmitter side as plotted in Fig. 1(b), which depicts the TX efficiency and data rate of recent transmitters for sensor applications with TX output power. FSK has broadly utilized with large modulation index (>1) since it has a faster response time than OOK [13]. Furthermore its constant envelope nature with zero crossing data permits use of an efficient nonlinear PA by directly modulating the oscillator [10], [15]–[17], and [19] or up-converting the baseband signal [13], [14], [18]. Nevertheless, the receiver architecture is more complex and consumes more power than envelope detector based architecture because it requires accurate local oscillator and I/Q signal path to demodulate the received signal [13]–[16], [18], and [20], [21].

With these observations in mind, we propose a low energy FSK transceiver using 902–928 MHz ISM band for BSN by combining only the strong points of OOK and FSK [22]. That is, the efficient direct modulation FSK transmitter and the simple envelope detector based receiver are employed. The reason why this is possible is that we adopt injection-locked frequency divider (ILFD) as frequency-to-amplitude converter in receiver mode and digitally-controlled oscillator (DCO) in transmitter mode. Thanks to the ILFD based transceiver architecture the receiver and transmitter consume 420 μW and 700 μW, respectively, at -10 dBm output power with a data rate of 5 Mb/s, corresponding to energy consumption of 84 pJ per received bit and 140 pJ per transmitted bit.

The rest of this paper is organized as follows. Section II describes the overall transceiver architecture. Then, Section III gives an analysis of injection locking properties which makes transceiver energy-efficient. Detailed designs of the building blocks are explained in Section IV. Section V discusses prototyped method for calibrating the frequency drift of DCO using injection locking and pulling phenomenon without the need for a frequency synthesizer. The measurement results will be shown in Section VI. Finally, Section VII concludes the paper.

II. Architecture Overview

Fig. 2 shows overall transceiver architecture which is composed of a MCU controller, a direct modulation FSK transmitter, and a simple envelope detector based receiver. The ILFD plays an important role in making the transceiver energy-efficient because it is used as frequency-to-amplitude converter and DCO in receiver and transmitter, respectively. In the receiver, the tuned LNA amplifies the received FSK signal. Through the ILFD, the LNA output is converted to amplitude modulated signal which is directly fed to the envelope detector, and then base band signal is quantized by 1-bit ADC. The ILFD makes it possible to reduce hardware complexity of FSK baseband circuits without accurate local oscillator and I/Q signal path. In addition, as explained in Section III, required LNA gain to overcome the sensitivity limitation of envelope detector is also mitigated because

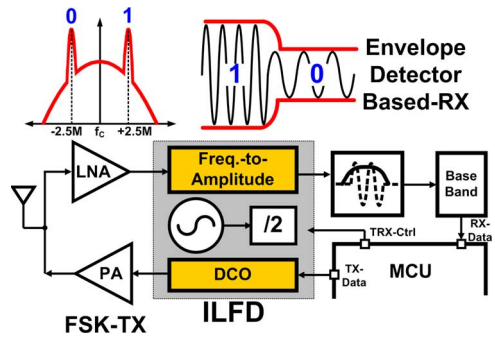

Fig. 2. Overall transceiver architecture.

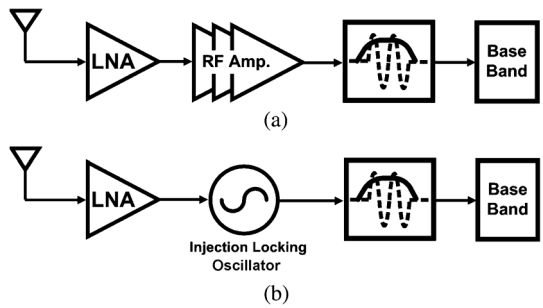

Fig. 3. Comparison of receiver architecture. (a) RF envelope detection. (b) ILFD based envelope detection.

ILFD, which is located between RF amplifier and envelope detector, can convey weak RF signal to strong full swing signal into envelope detector. Since the RF amplifier consumes most of power in such receiver architecture, in terms of power consumption, ILFD based receiver used in FSK demodulation has the advantage over the conventional envelope detector based receiver used in OOK demodulation.

In the transmitter, the ILFD is utilized as DCO and the FSK data is transmitted by directly modulating the DCO with TX data using efficient switching PA. Especially the DCO replaces frequency synthesizer to reduce power consumption and to eliminate the XO. Removal of XO with fast stabilization time allows more efficient duty cycling operation, which leads to low energy consumption. On the other hand, because DCO is not phase-locked to stable reference oscillator, it has low frequency stability and suffers from frequency drift over temperature variation. To calibrate frequency drift of DCO, the ILFD is exploited as well. Through ILFD, the desired control code of DCO can be periodically corrected by detecting whether injection locking occurs or not, as discussed in Section V.

III. Injection-Locking in Transceiver

A. Envelope Detection Based Architecture

The most energy-efficient way to implement receiver is to adopt envelope detector in receiver chain as shown in Fig. 3. Fig. 3(a) and (b) show conventional RF envelope detection architecture and proposed ILFD based architecture, respectively. In conventional architecture, high RF gain is required for envelope detector to properly function due to the nonlinear nature of

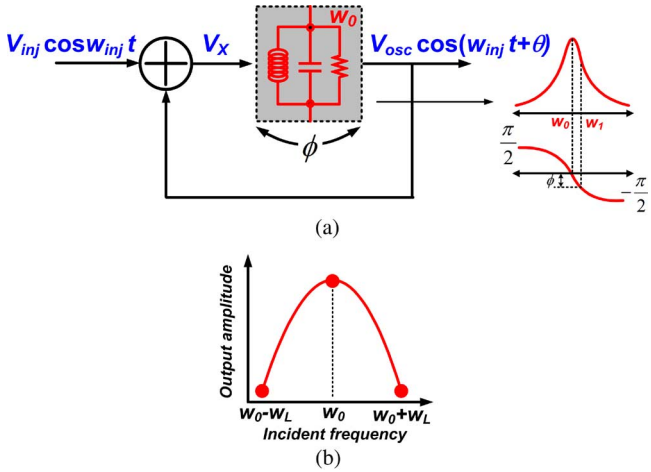

Fig. 4. Frequency-to-amplitude conversion of ILO. (a) Conceptual diagram. (b) Oscillation amplitude.

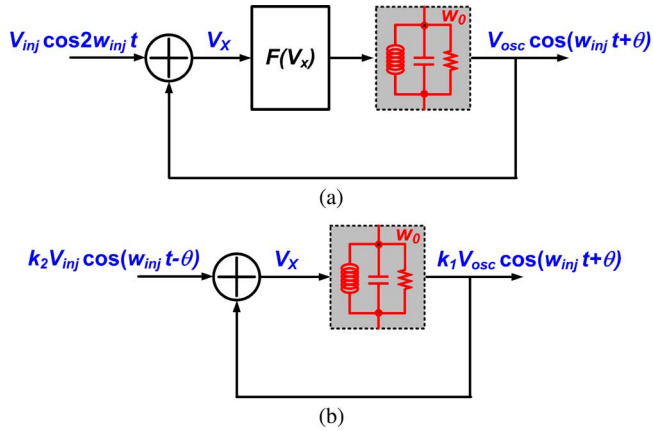

Fig. 5. Frequency-to-amplitude conversion of ILFD. (a) Conceptual diagram. (b) Equivalent conceptual diagram of (a).

the envelope detection process, and the RF input must be amplified to approximately 100 mV. From the analysis of [12], increasing gain in the front-end of an envelope detection receiver has the advantage over enhancing front-end noise performance. However, the available RF gain is limited and requires too much power consumption.

In Fig. 3(b), instead of RF amplifier, oscillator is located between LNA and envelope detector for the purpose of using the injection locking concept. Because strong full swing signal of oscillator isolates LNA from envelope detector, the sensitivity limitation and noise generation from envelope detector cannot influence on front-end of receiver. Therefore, the RF gain can be reduced by injection-locking the oscillator. To compare with RF envelope detection architecture, assuming that the amplitude of the injected voltage ($V_{\rm inj}$) is much smaller than the amplitude of the free-funning oscillator ($V_{\rm osc}$), the locking range can be approximated by

$$w_L \approx \frac{w_0}{2Q}\frac{V_{\rm inj}}{V_{\rm osc}} \tag{1}$$

where ω_L is locking bandwidth and ω_0 is operating frequency, and Q is the quality factor of oscillator [23]. The oscillator can be locked from $\omega_0 - \omega_{\rm L}$ to $\omega_0 + \omega_{\rm L}$. For example, in this application, the receiver's oscillator has a free-running differential peak-to-peak swing of 0.7 V and a tank inductor with $Q = 10$. For the value for $\omega_L = 2.5$ MHz, the injected signal into the oscillator will have swing of 35 mV, which is smaller than the case of Fig. 3(a). Therefore, ILFD based architecture enables to reduce power consumption of front-end circuits.

B. Frequency-to-Amplitude Conversion

The proposed injection-locked FSK transceiver is based on the property that the incident frequency of injection locked oscillator (ILO) can be discriminated by ILO's output amplitude, which means frequency-to-amplitude conversion. Following the analysis in [23], the conceptual diagram of ILO with LC tank which resonates at ω_0 and has a quality factor of Q is shown in Fig. 4(a). Now suppose that the ILO oscillates at ω_1 $(= \omega_{\rm inj})$ and injection locking occurs by proper injection signal. The output is represented by a phase-modulated signal having a carrier frequency of $\omega_{\rm inj}$. For simplicity, we assume $V_{\rm inj}$ is much smaller than $V_{\rm osc}$ and the output amplitude of ILO is proportional to V_X. The V_X is equal to

$$\begin{aligned} V_X &= V_{\rm inj}\cos(w_{\rm inj}t) + V_{\rm osc}\cos(w_{\rm inj}t+\theta) \\ &= (V_{\rm inj} + V_{\rm osc}\cos\theta)\cos(w_{\rm inj}t) - {\rm V}_{\rm osc}\sin\theta\sin(w_{\rm inj}t) \\ &= \sqrt{V_{\rm osc}^2 + V_{\rm inj}^2 + 2V_{\rm osc}V_{\rm inj}\cos\theta}\cos(w_{\rm inj}t+\varphi) \\ &\approx V_{\rm osc}\cos(w_{\rm inj}t+\varphi). \end{aligned} \tag{2}$$

We define

$$\tan\varphi = \frac{V_{\rm osc}\sin\theta}{V_{\rm inj} + V_{\rm osc}\cos\theta}. \tag{3}$$

The V_X experiences a phase shift of LC tank

$$\begin{aligned} V_{\rm osc}\cos(w_{\rm inj}t+\theta) = V_{\rm osc}\cos\Big(w_{\rm inj}t+\varphi \\ + \tan^{-1}\left[\frac{2Q}{w_0}\left(w_0 - w_{\rm inj} - \frac{d\varphi}{dt}\right)\right]\Big) \end{aligned} \tag{4}$$

and

$$\begin{aligned} \tan(\theta-\varphi) &= \frac{V_{\rm inj}\sin\theta}{V_{\rm osc} + V_{\rm inj}\cos\theta} \\ &\approx \frac{V_{\rm inj}}{V_{\rm osc}}\sin\theta. \end{aligned} \tag{5}$$

Therefore, from (2), (3), (4), and (5),

$$\frac{d\theta}{dt} = w_0 - w_{\rm inj} - \frac{w_0}{2Q}\frac{V_{\rm inj}}{V_{\rm osc}}\sin\theta. \tag{6}$$

For the oscillator to lock to the input, the phase difference, θ, should remain constant with time, yielding the following condition under injection locking:

$$w_0 - w_{\rm inj} = \frac{w_0}{2Q}\frac{V_{\rm inj}}{V_{\rm osc}}\sin\theta. \tag{7}$$

Then the phase difference between $V_{\rm osc}$ and $V_{\rm inj}$ reaches $-\pi/2$ and $\pi/2$ at the edges of the locking range $(\omega_{\rm L})$. In the locking range, the output amplitude of ILO is given by

$$\sqrt{V_{\rm osc}^2 + V_{\rm inj}^2 + 2V_{\rm osc}V_{\rm inj}\cos\theta}. \tag{8}$$

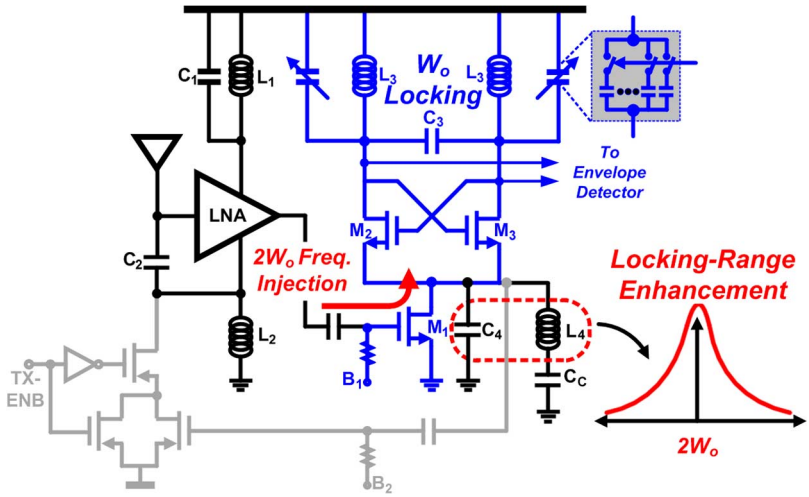

Fig. 6. Schematic of receiver front-end.

Fig. 4(b) plots the output amplitude of ILO with respect to incident frequency in the locking range. As shown in Fig. 4(b), the frequency-to-amplitude conversion property of ILO can be exploited in the frequency range of $\omega_0 - \omega_L$ to ω_0 or from ω_0 to $\omega_0 + \omega_L$.

Fig. 5(a) shows the conceptual diagram of ILFD with *LC* tank and nonlinear function based on [24]. The block $F(V_X)$ models the all the nonlinearities in the oscillator. For the divided-by-2 function and $F(V_X) = a_0 + a_1 V_X + a_2 V_X^2 + a_3 V_X^3$, the frequency components of $2\omega_{inj}$ and $3\omega_{inj}$ are filtered out, so only the frequency component of ω_{inj} is fed back to adder. Fig. 5(b) depicts the equivalent functional diagram of Fig. 5(a). Except for scaling factor, the behavior of ILFD is the same as that of ILO. In terms of circuit implementation, since the ILFD is more feasible than the ILO, the ILFD is adopted to obtain frequency-to-amplitude conversion property. It makes possible to use an energy-efficient envelope detection receiver.

IV. Transceiver Implementation

A. Receiver Front-End

The receiver front-end serves two roles: amplifying weak received signals with LNA and converting frequency-modulated signals to amplitude-modulated signals with ILFD. Fig. 6 shows the receiver front-end schematic focused on ILFD, the frequency-to-amplitude converter. The LNA with a tuned L_1C_1 load amplifies the received FSK signal, and L_2C_2 tank is used for 50 Ω input impedance matching with antenna. The differential negative-G_m oscillator forms the core of the ILFD. The incident signal of frequency $2W_0$ is injected on the gate of M_1, which delivers the incident signal to the common source connection of M_2 and M_3. Switching M_2 and M_3 at a rate of the oscillation frequency forms a mixer that translates injected signal of frequency $2W_0$ to injection locking signal of frequency W_0. The ILFD with L_3C_3 tank should oscillate around at half of the incident frequency. In addition, the L_4 is introduced to resonate with C_4, which is composed of parasitic capacitance (C_{gd} and C_{db} of M_1 and C_{sb} of M_2 and M_3) and intentionally added capacitor for tuning at incident frequency to enhance the locking range of ILFD [25]. The C_C, in series with L_4, serves as a dc block. The amplitude-modulated ILFD output signal is then applied to the next stage, the energy-efficient envelope detector.

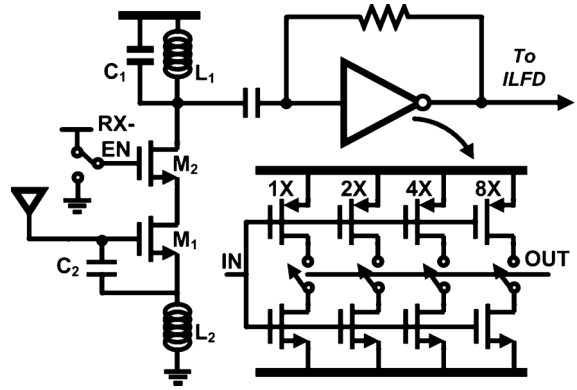

Fig. 7. Schematic of LNA.

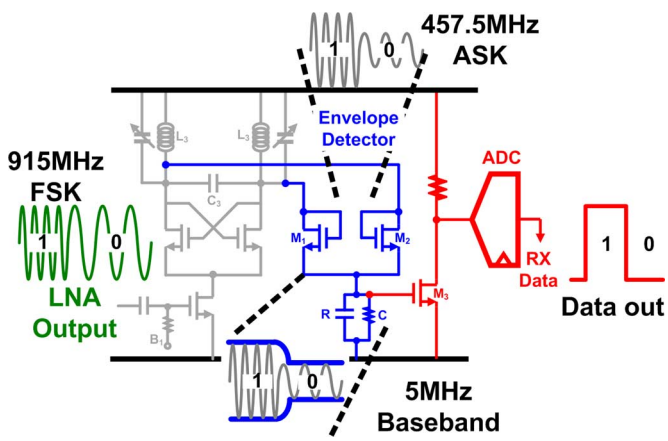

Fig. 8. Schematic of receiver baseband.

Because locking range of ILFD is mainly determined by the injected power, the LNA gain should be high enough to maintain its operating frequency range for minimum input power. Furthermore, since the noise of the front-end entering the ILFD

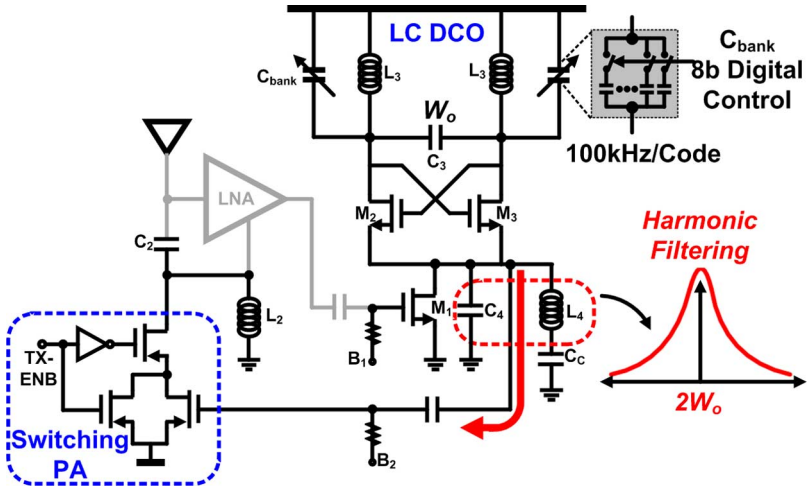

Fig. 9. Schematic of transmitter.

is integrated across the entire RF bandwidth, the narrow RF filtering at the LNA is required. To satisfy both of these requirements, the LNA consists of the tuned amplifier cascaded with inverter based amplifier as described in Fig. 7. The M_1 transistor is inductively degenerated to provide 50 Ω input resistance at 920 MHz. The L_1C_1 and L_2C_2 tanks in combination with L_4C_4 tank in Fig. 6 provide the narrow bandwidth RF filter. The 4 bit coded variable width inverter with resistive feedback can adjust overall front-end gain. As a result, the voltage gain of the LNA can be adjusted up to 40 dB with 30 MHz bandwidth while consuming 280 μA from the 0.7 V supply.

All inductors in Fig. 6 are low-cost off-chip devices with Q-factor less than 13. While external inductor is a high cost, it has a high Q-factor compared with on-chip inductor, which makes it possible to reduce the bias current of the LC oscillator for starting the oscillation. Because inductance can be spread in the off-chip inductor, the digitally controlled capacitor banks are utilized with all inductors in order to adjust resonance frequency of LC tanks.

B. Receiver Baseband

From the output of the ILFD, receiver baseband demodulates the amplitude-modulated signal using an envelope detector, a baseband amplifier, and an 1-bit ADC as depicted in Fig. 8. The output amplitude of the envelope detector is mapped to the output amplitude of the ILFD by diodes M1, M2 and R (80 kΩ) C (5 pF) low-pass filter. The envelope detector is implemented with a differential pair biased in weak inversion region with 5 μA of current for nonlinearity. For a given amplitude-modulated signal, the minimum level of the change in output voltage can be influenced by output noise power of the envelope detector. The output noise of envelope detector is about 140 μV_{rms} or 400 μV_{pp}, and therefore, the envelope detector output should have amplitude greater than approximately 4 mV_{pp}, for the correct operation in SNR of 20 dB. On the other hand, owing to the strong injection-locked signal from ILFD, the envelope detector noise has a negligible effect on noise figure of the receiver chain. Through envelope detector, the amplitude-modulated signal is converted to DC baseband signal which is fed to the simple common source amplifier. The ADC following the baseband amplifier 1 bit-quantizes the baseband signal, and it is implemented with a comparator which has a digitally configurable offset voltage that set the differential input voltage threshold. All the baseband circuits are biased in subthreshold region and consume only 14 μW.

C. Transmitter

The schematic of the transmitter is shown in Fig. 9. The transmitter generates a 5 Mb/s FSK signal by directly modulating the DCO with efficient nonlinear switching PA. In this case, the ILFD with programmable capacitor bank C_3 and inductor L_3 is utilized as DCO which employs differential negative-G_m oscillator. In the absence of the incident signal, the common source node of M_2 and M3 oscillates at twice the frequency of the output signal of ILFD, which makes it an appropriate output node for transmitting operation. Because the common source node of M_2 and M_3 contains all kinds of harmonic frequencies of the fundamental frequency which are generated by L_3C_3 tank, in transmitter mode, L_4C_4 tank is adopted to filter out any harmonic frequencies but the second harmonic, resonating at double the DCO fundamental frequency.

The DCO can be tuned of a desired frequency with 100 kHz accuracy by 8 bit capacitor bank and the frequency drift over 60 degree temperature variation can be periodically compensated by prototyped frequency calibration method thanks to ILFD based architecture. The DCO phase noise is -120 dBc/Hz at 1 MHz offset, and the stabilization time is less than 500 ns, shorter than three bit periods, which enables the transceiver to operate with efficient duty cycling operation. The PA uses a cascode transistor to improve isolation between the antenna and DCO, and reuses the L_2C_2 tank for the load impedance to effectively drive antenna. The transmitter consumes 700 μW at the output power of -10 dBm and the output power level is adjustable by controlling bias point of B_2. The TX transmits data efficiently, due to its nonlinear switching PA.

V. Frequency Calibration Method

The body sensor network system consists of sensor nodes which collect the vital signal, and the base station which manages sensor nodes. In such a system, it is critical that the sen-

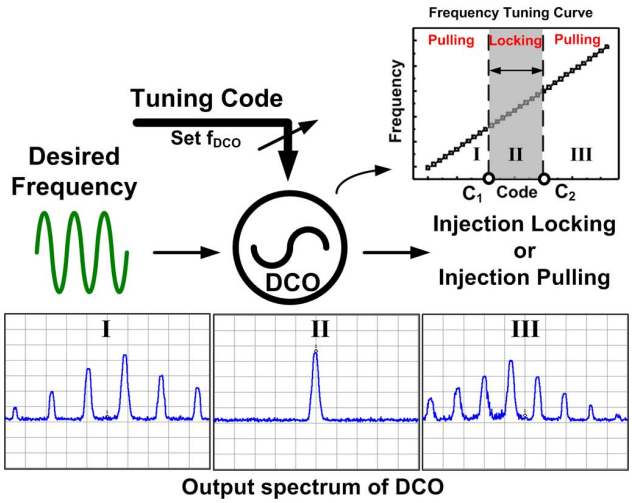

Fig. 10. Conceptual diagram of frequency calibration.

sors consume minimal power in order to preserve battery life time while the corresponding base station is free to consume much more power. Therefore, by shifting complexity and communication power in the sensor network from sensors to base station, the energy consumption of sensor nodes can be significantly minimized. Instead of using a frequency synthesizer in the transceiver, the ILFD is utilized as DCO and it replaces frequency synthesizer to reduce power consumption and to eliminate the XO. Still, open loop DCO has low frequency stability and suffers from frequency drift over temperature variation because it is not phase-locked to stable reference oscillator. To calibrate the drift of the open loop DCO, the new calibration method is proposed using ILFD based receiver architecture. In the proposed system, after the base station which has PLL with crystal oscillator wirelessly sends accurate frequency signal periodically, sensor nodes are injection-locked to the frequency signal, and then frequency calibration is performed. The implementation of such a system is prototyped without any help of external measurement equipment or devices to monitor the drift of DCO.

Fig. 10 shows the conceptual diagram of frequency calibration method. The purpose of calibration is setting the DCO tuning code to desired frequency. In order to calibrate the DCO, first, inject external accurate/fixed frequency signal into DCO. Second, tune the DCO control code from the lowest value to the highest value. Third, find the code value, C_1, which makes the DCO operate from injection pulling mode to injection locking mode. Then, find the code value, C_2, which makes the DCO oscillate in locking into pulling. Finally, average the C_1 and C_2. The frequency of the DCO, coded with average value of the C_1 and C_2, is the frequency that we target.

Because the locking range of oscillator is determined by operating frequency, amplitude of free-running oscillator, amplitude of injected signal, and the Q-factor of oscillator, if all the factors are constant by using external fixed frequency signal, the locking range is also constant. In the case of Fig. 10, with the desired frequency (ω_0) and locking range of DCO (ω_{L}), the frequency range of the free-running DCO, which can be locked to

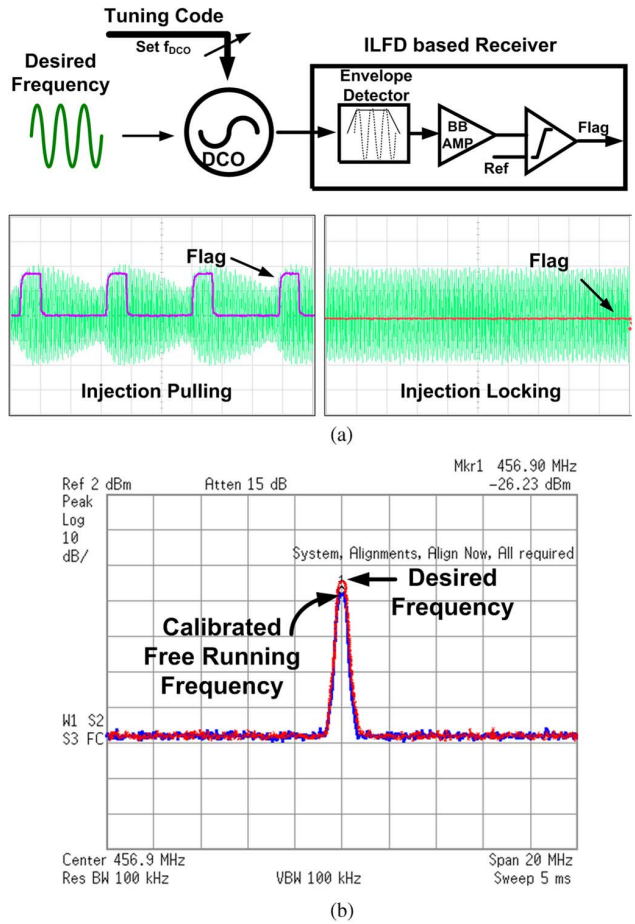

Fig. 11. Implementation of frequency calibration. (a) Implementation with ILFD based receiver. (b) Calibration result.

desired signal, is between $\omega_0 - \omega_{\mathrm{L}}$ and $\omega_0 + \omega_{\mathrm{L}}$. Since the symmetry of locking range in injection locking phenomenon, the DCO can be calibrated by finding the edge of the locking range. From region I to region III, the DCO's tuning code is increased and the output spectrum of DCO is varied as shown in Fig. 10.

With this calibration concept, in order to get the tuning code of C1 and C2, the implementation for detecting whether injection locking occurs or not is the key. Fig. 11(a) presents the implementation of proposed calibration method. With injection of desired frequency, the output of the DCO, tuned by certain code, is monitored by the same structure of receiver baseband. As shown in Fig. 10, if injection pulled, the output spectrum of the DCO is not one tone signal but multi-tone signal. Likewise, the output signal of the DCO is amplitude-modulated even though one tone signal is injected to the DCO. Therefore, the envelope detector with programmable comparator can be exploited to discriminate whether injection pulling is occurred or not. The measured waveforms of Flag node are presented in Fig. 11(a) with output signal of DCO. Before transceiver transmits the data, in calibration mode, without any hardware and power overhead, the DCO tuning frequency can be correctly tuned by its ILFD based architecture. Fig. 11(b) shows that the spectrum of calibrated free-running DCO with injection-locked desired frequency by using proposed method. In this measurement, the 913.8 MHz signal is applied to ILFD to lock DCO at

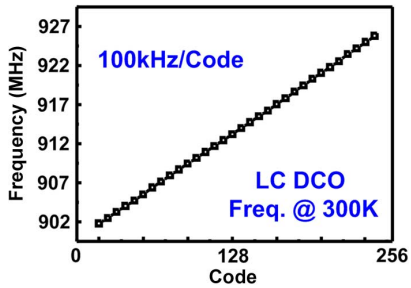

Fig. 12. DCO frequency tuning curve.

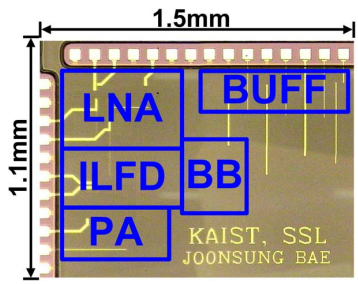

Fig. 13. Chip microphotograph.

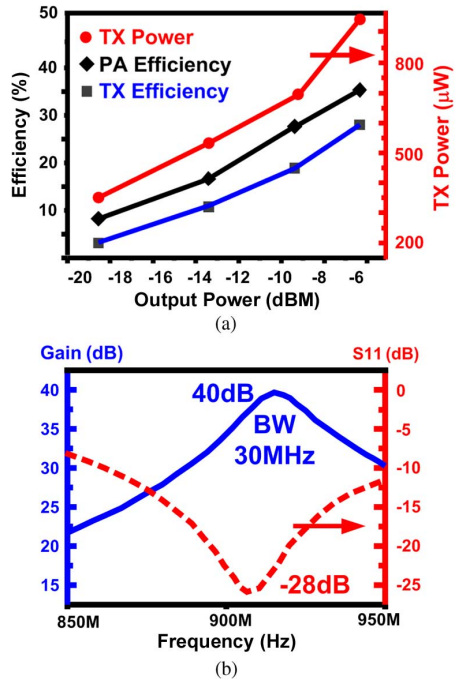

Fig. 14. Performance of antenna interfacing circuits. (a) Transmitter and PA efficiency. (b) S11 and gain curves of LNA.

456.9 MHz, and the frequency difference between free-running oscillator and 456.9 MHz is less than 100 kHz.

The frequency stability is affected by frequency tuning step size. Fig. 12 plots the DCO frequency with tuning code. The DCO frequency can be tuned of a desired frequency over the range of 902–927 MHz with 100 kHz accuracy by 8-bit coded capacitor bank. At a bit rate of 5 Mb/s and assuming 256 bits are needed for each calibration cycle, it takes about 50 μs to calibrate the frequency drift of DCO. From the studies on human gait [26], frequency drift can result from human motion and calibration should be repeated every 100 ms. The energy overhead of calibration on the human body is less than 0.1%. As a result, the frequency synthesizer is removed by the open loop DCO with 100 ppm frequency stability, which has a negligible effect on overall performance of the transceiver.

VI. Implementation Results

The ILFD based FSK transceiver has been fabricated in 0.18 μm mixed-mode CMOS technology and its chip microphotograph is shown in Fig. 13. The total chip area including pads is 1.1 $\times$1.5 mm^2. The five inductors used in the transceiver are off-chip devices whose Q-factor is higher than that of an on-chip inductor. All circuit measurements are performed with a 0.7 V supply.

Fig. 14 plots the performance of antenna interfacing circuits, PA and LNA. The output power of Fig. 14(a) is from the second harmonic frequency of the DCO. The difference of transmitted power between the fundamental harmonic and the second harmonic from the DCO is more than 60 dB. The output power is currently set to -10 dBm with TX efficiency of 15%, and its power level can be raised up to -6 dBm to compensate for the antenna loss and improve TX efficiency. Due to efficient switching operation of the nonlinear PA, the TX efficiency is more than 35% at the operating point where the TX outputs -6 dBm as shown in Fig. 14(a). Fig. 14(b) is the measured S11 of the LNA and gain curves as a function of the frequency. The return loss of the inductively degenerated LNA is less than -15 dB over the 880–940 MHz, which contains 902–928 MHz ISM band. The tuned LNA cascaded with resistive feedback inverter amplifier gives voltage gain up to 40 dB with 30 MHz RF bandwidth.

Fig. 15 shows the output spectrums of (a) TX and (b) ILFD. The 5 Mb/s BFSK transmitted signals with frequency deviation of 5 MHz, which has modulation index of 1, are measured by a spectrum analyzer. Fig. 15(b) describes output spectrum of ILFD signals by using 50 Ω matched output buffer (test PA). To observe the output amplitude of ILFD by measurement equipment such as spectrum analyzer and oscilloscope, the test buffer is implemented with linear PA as well. The spectrum shows divided by two signals from transmitted signal, which is shown in Fig. 15(a). With transmitted signal, which has data rate of 5 Mb/s and frequency deviation of 5 MHz, the ILFD is injection locked to amplitude modulated signal, which contains data rate of 5 Mb/s and frequency deviation of 2.5 MHz. In the same manner, when the signal of 2.5 Mb/s data rate and 5 MHz frequency deviation is injected to ILFD, the output of ILFD shows FSK signal of 2.5 Mb/s data rate and 2.5 MHz frequency deviation. The two signals are superimposed in Fig. 15(b). Although the injection locked signals are frequency modulated, higher the frequency, stronger the received signal.

Fig. 16 shows measured time-domain signals for the receiver chain. When a high frequency signal is received, the output amplitude of ILFD is high as shown in Fig. 16(a). The waveforms of Fig. 16(a) are also obtained by using test buffer. Because of negative gain of baseband circuits, the data one and data zero are inverted in measurement result. On average, when a data 1 and 0 are received at RF input power of -60 dBm, amplitude of ILFD is 47.2 mV and 49.6 mV, respectively. The eye diagram

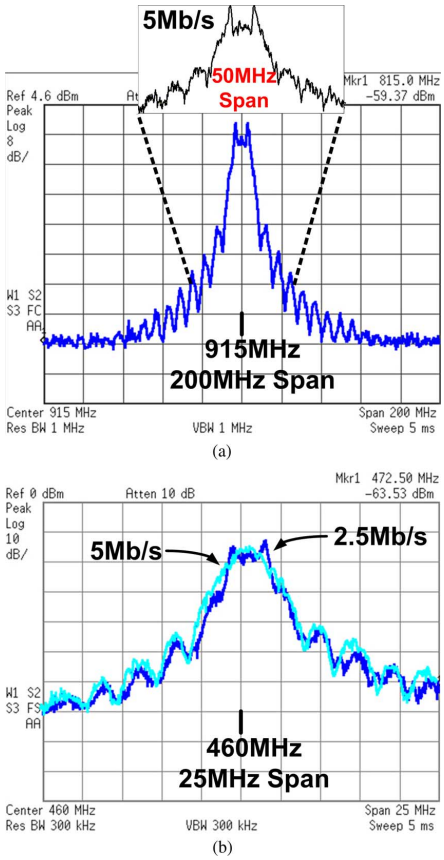

Fig. 15. Output spectrums of (a) transmitter and (b) ILFD.

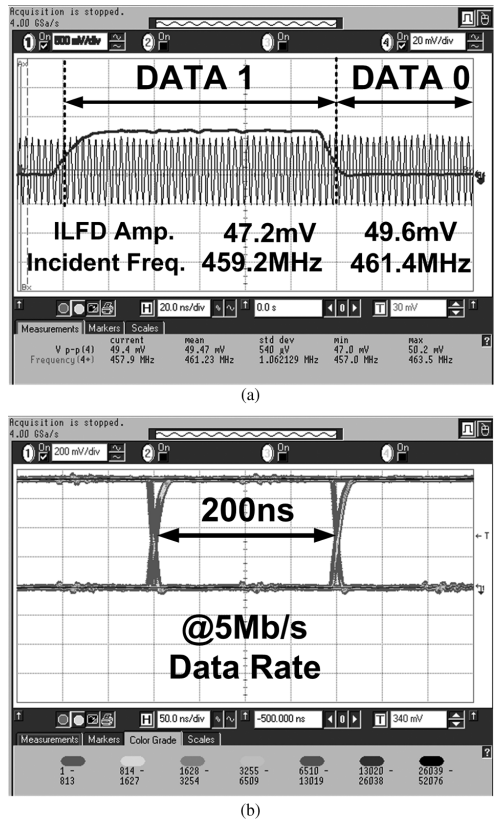

Fig. 16. Receiver time domain signals. (a) ILFD output and demodulated data. (b) Eye diagram of demodulated bit streams.

of the demodulated bit streams at RF input power of -70 dBm is shown in Fig. 16(b). The 5 Mb/s and 2^7-1 PRBS data is applied to the TX side to draw the eye diagram. Even though input power of -70 dBm is applied to the receiver chain, there is almost no jitter in the demodulated signal. In general, the frequency transition response in injection locking oscillator is determined and limited by its locking range. Because with LNA gain of 40 dB and the 8 dB gain of the M_1 with $\mathrm{L}_4\mathrm{C}_4$ tank in Fig. 6, the -70 dBm input signal is amplified and then applied to ILFD with measured locking range over 5 MHz, the demodulated data does not suffer from jitter problem. However, if weak input signal is received, the received data will encounter jitter problem with limited locking range, which gives inter-symbol interference. In this design, the receiver sensitivity is not limited by RF front-end noise figure but locking range of 5 MHz.

To compare with predicted locking range, the locking range of ILFD can be expressed as the following equation [23]:

$$w_L \approx \frac{w_0}{2Q}\frac{4}{\pi}\frac{V_{\mathrm{inj}}}{V_{\mathrm{osc}}}. \tag{9}$$

The operating frequency ω_0 is 920 MHz, and the Q-factor of ILFD is 9, the amplitude of injected signal of -22 dBm is approximately 50 $\mathrm{mV_{pp}}$, and the amplitude of the oscillator is approximately 1.2 $\mathrm{V_{pp}}$. The calculated locking range $2\,\omega_{\mathrm{L}}$ of 5.4 MHz closely matches the measured locking range. In this case, the amplitude of the envelope detector output is 35 $\mathrm{mV_{pp}}$, which is larger than minimum level of output amplitude of the envelope detector, 4 $\mathrm{mV_{pp}}$.

TABLE I
POWER BREAKDOWN OF TRANSCEIVER

Receiver	
LNA	280μA
ILFD	300μA
Baseband	20μA
Total Power	420μW
Transmitter	
DCO	300μA
PA	700μA
Total Power	700μW

The oscillation amplitude of the ILFD measured by the test buffer is plotted in Fig. 17 as a function of the incident frequency for different incident power. The locking range is determined by the frequency difference between the two ends of each curve. It increases with incident power. The amplitude of ILFD is also raised with incident frequency. But the mapping between output amplitude of ILFD and incident frequency is not symmetric, as explained in Section III-B. It is thought that the phase difference between incident signal and oscillation signal is not $\pi/2$ or $-\pi/2$ at the edge of the locking range in all cases because we assume V_{inj} is much smaller than V_{osc}, for simplicity. Or, it is plausible that the frequency dependency of test buffer affects the measurement results. The method for compensation of the relationship between incident frequency and output amplitude of injection locking oscillator can be supplement with

TABLE II
PERFORMANCE SUMMARY AND COMPARISON

Reference	[11] MIT, JSSC'07	[12] Berkely, JSSC'09	[8] Berkely, ISSCC'05	[16] Berkely, JSSC'06	[19] KASIT, VLSI'09	This Work
Technology	0.18μm	90nm	0.13μm	0.13μm	0.18μm	0.18μm
Supply	1.4V	0.5V	0.9V	0.4V	0.7V	0.7V
Modulation	OOK	OOK	OOK	FSK	FSK	FSK
Freq. Band	916.5MHz	2GHz	1.9GHz	2.4GHz	400MHz	920MHz
RX Sensitivity	-37dBm	-72dBm	-100.5dBm	N/A	-70dBm	-73dBm
Data Rate	1Mb/s	100kb/s	5kb/s	300kb/s	250kb/s	5Mb/s
TX P_{out}	-11.4dBm	-	250μW	300μW	-16dBm	-10dBm
Power Consumption	RX : 500μW TX : 3.8mW	52μW	RX : 400μW TX : 1.6mW	RX :330μW TX : 1.0mW	RX :490μW TX : 400μW	RX :420μW TX : 700μW
Energy/bit (RX)	0.5nJ/b	0.52nJ/b	80nJ/b	1.1nJ/b	1.96nJ/b	84pJ/b
# of off-chip comp.	2	1	1	0	4	5
Application	WSN	Wake-up RX	WSN	WSN	Implant WSN	WBSN

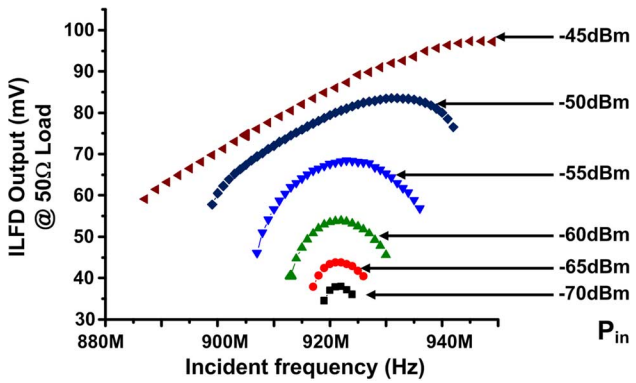

Fig. 17. Oscillation amplitude of the ILFD as a function of incident frequency.

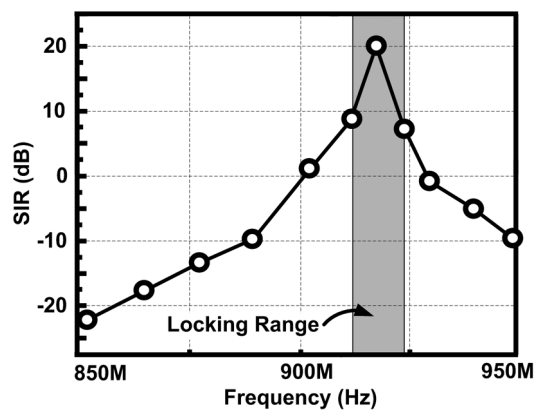

Fig. 18. Signal-to-interferer ratio (SIR) performance.

monitoring the received power as a further work. From the measurements, the frequency-to-amplitude conversion property of ILFD is verified and it enables energy efficient transmitter and envelope detector based receiver architecture.

Fig. 18 shows the receiver's immunity to blocker near the 915 MHz ISM band. For the interference performance measurement, the bit rate is set to 5 Mb/s, the input signal to receiver is set to +6 dB above the sensitivity limit (−66 dBm), and the continuous wave blocker power is swept for each frequency until the BER is degraded to 0.1%. It gives signal-to-interference ratio (SIR) at each frequency, which represents the maximum interferer power level that can be tolerated without blocking the receiver. As plotted in Fig. 18, the receiver is quite vulnerable to blocker in the frequency range of locking range because the blocker could lock the ILFD as well. On the other hand, for the far off blockers, interferer performance is dominated by the filtering of the RF font-end. The SIR at the fundamental frequency of ILFD (460 MHz) and the fourth harmonic frequency of ILFD (1840 MHz) is less than −40 dB and −60 dB, respectively.

A power breakdown of the transceiver is presented in Table I. The total power consumption for the receiver and the transmitter are 420 μW and 700 μW, respectively, with −10 dBm output power. Table II summarizes major performance parameters of the proposed transceiver and compares them with the recent low energy transceivers.

VII. CONCLUSION

This work presents an energy-efficient 920 MHz FSK transceiver based on ILFD for wireless body sensor applications. For low energy consumption of the transceiver, the ILFD is adopted as frequency-to-amplitude converter in receiver mode, and as a DCO in transmitter mode. In the receiver, the ILFD reduces power consumption of FSK baseband circuits as well as RF amplifier. Thanks to the simplified hardware, receiver dissipates only 420 μW. In the transmitter, the ILFD, as a DCO, transmits FSK data with nonlinear switching PA, without any data rate limitation. The crystal-less open loop DCO accelerates on/off time within 500 ns and the transmitter consumes 700 μW at −10 dBm output power with a data rate of 5 Mb/s. The frequency drift of the DCO over 60 degree temperature variations can be periodically compensated by prototyped frequency calibration method thanks to ILFD based architecture. As a result, the transceiver implemented with 0.18 μm CMOS consumes 84 pJ per received bit and 140 pJ per transmitted bit, which achieves the most energy-efficient performance compared with state-of-the-art works.

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